Platform Conference

Direction • Design • Perspective • Analysis

# Addressing System Interface Requirements with HyperTransport™ Standards & APEX II™ Devices

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Product Marketing

January 2002


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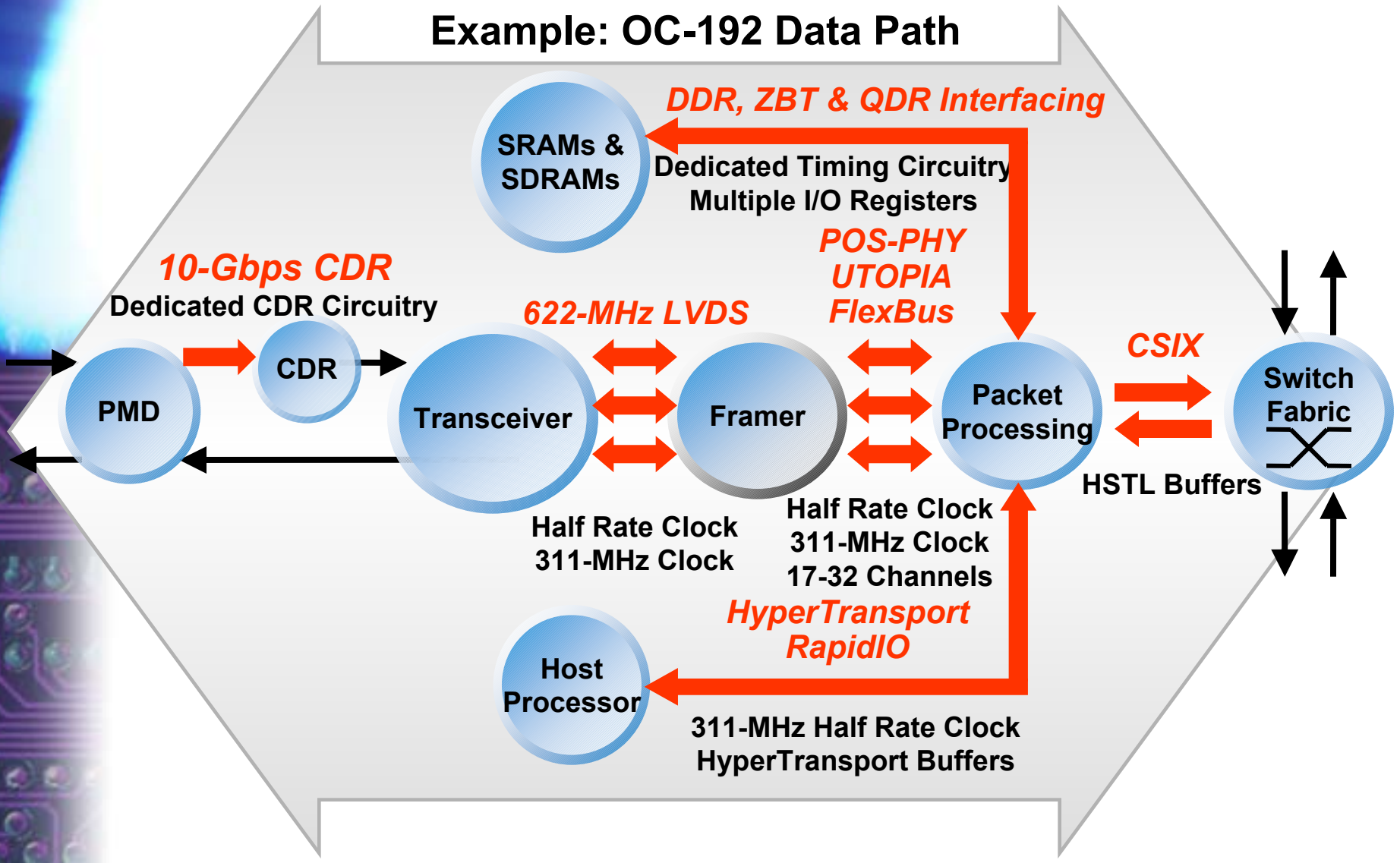
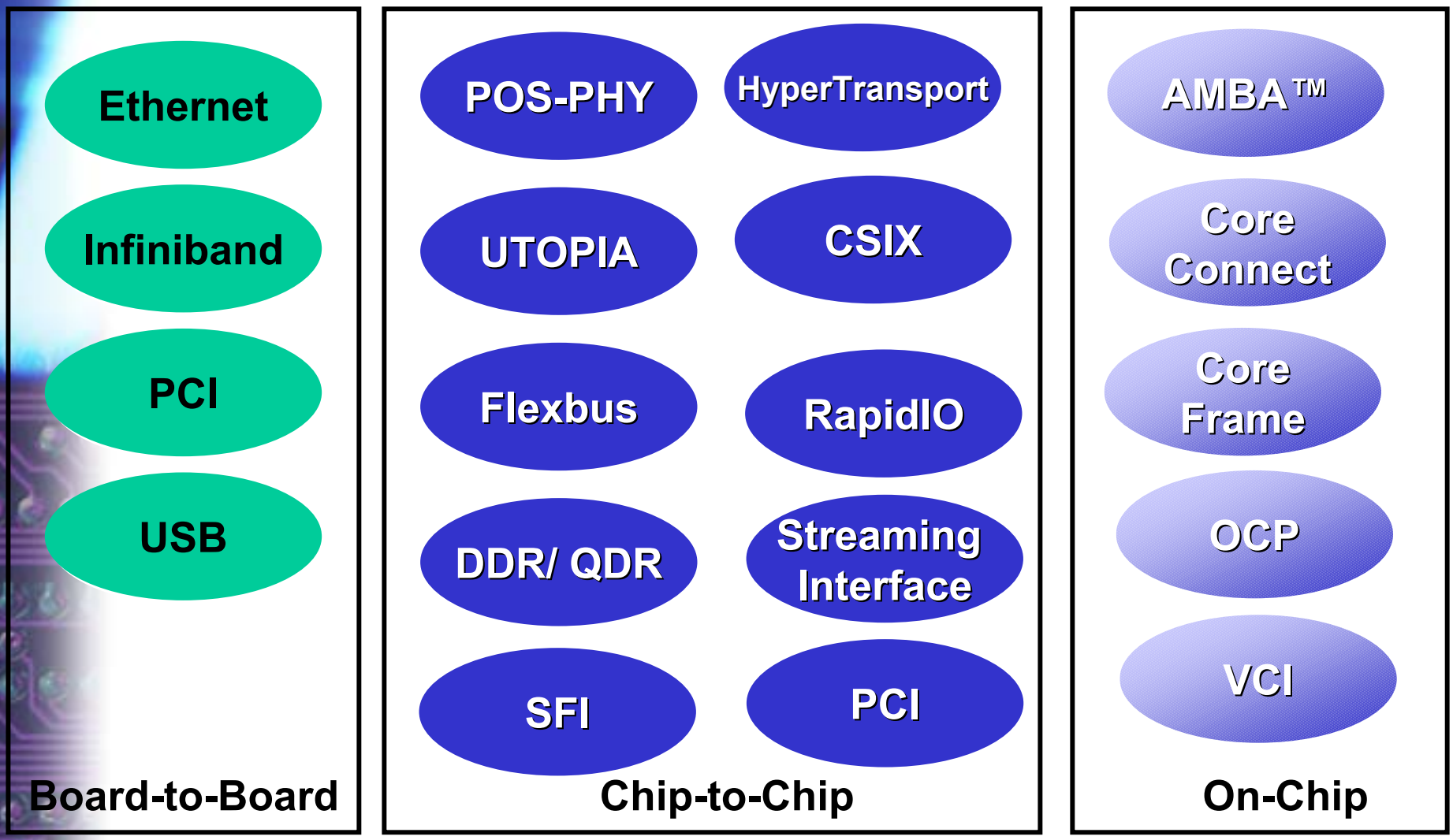
# Typical Communications Data Path



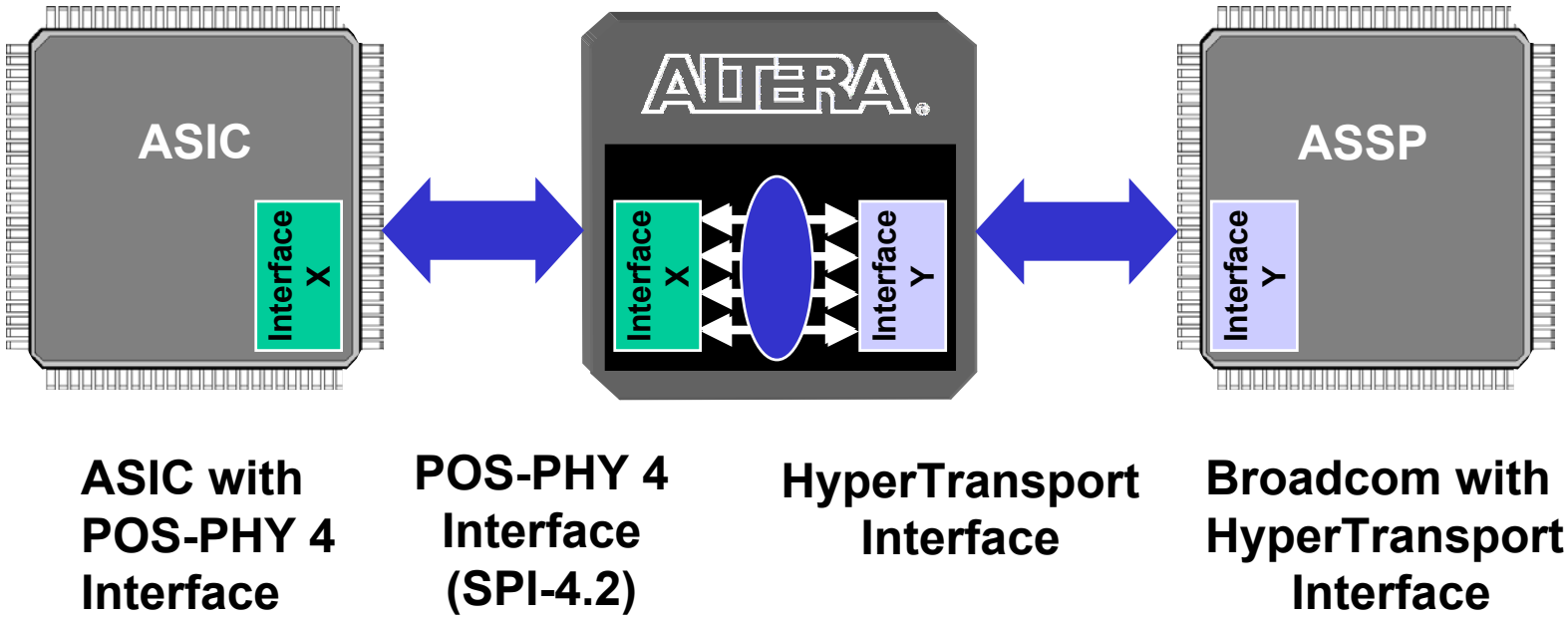
# Increasing Interfaces



# Bridging Interfaces with Altera

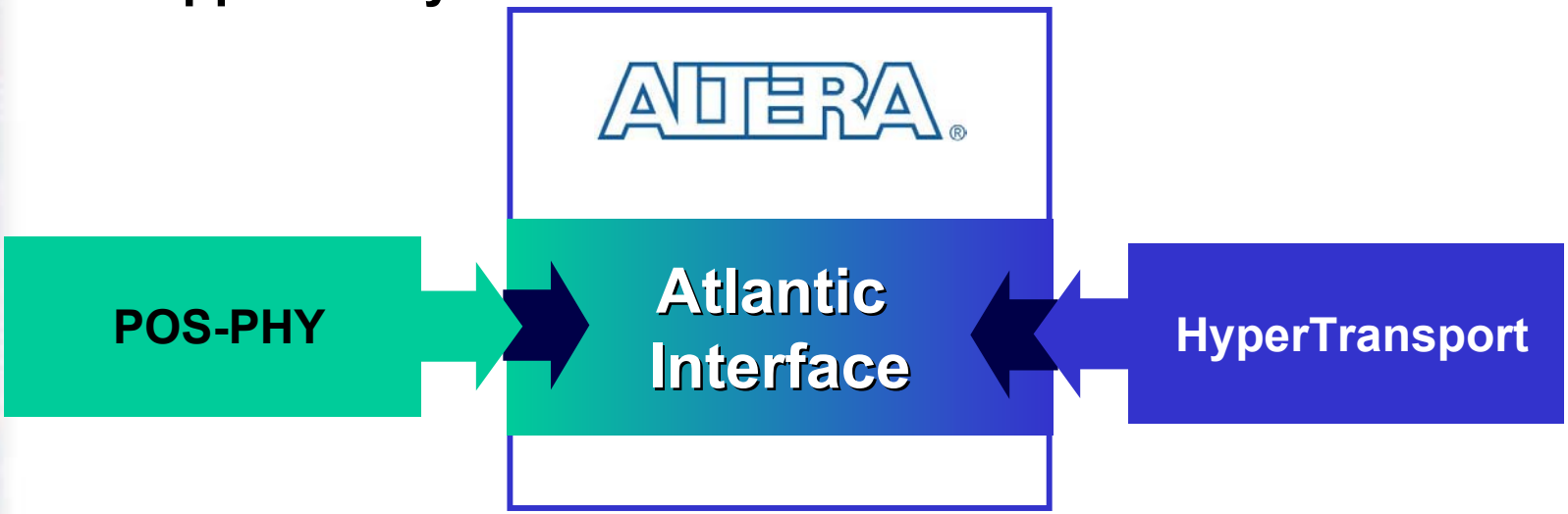
- Multiple Interfaces on Board
- Bridges Needed between Different Interfaces

## Example: POS-PHY Level 4 to HyperTransport Bridge



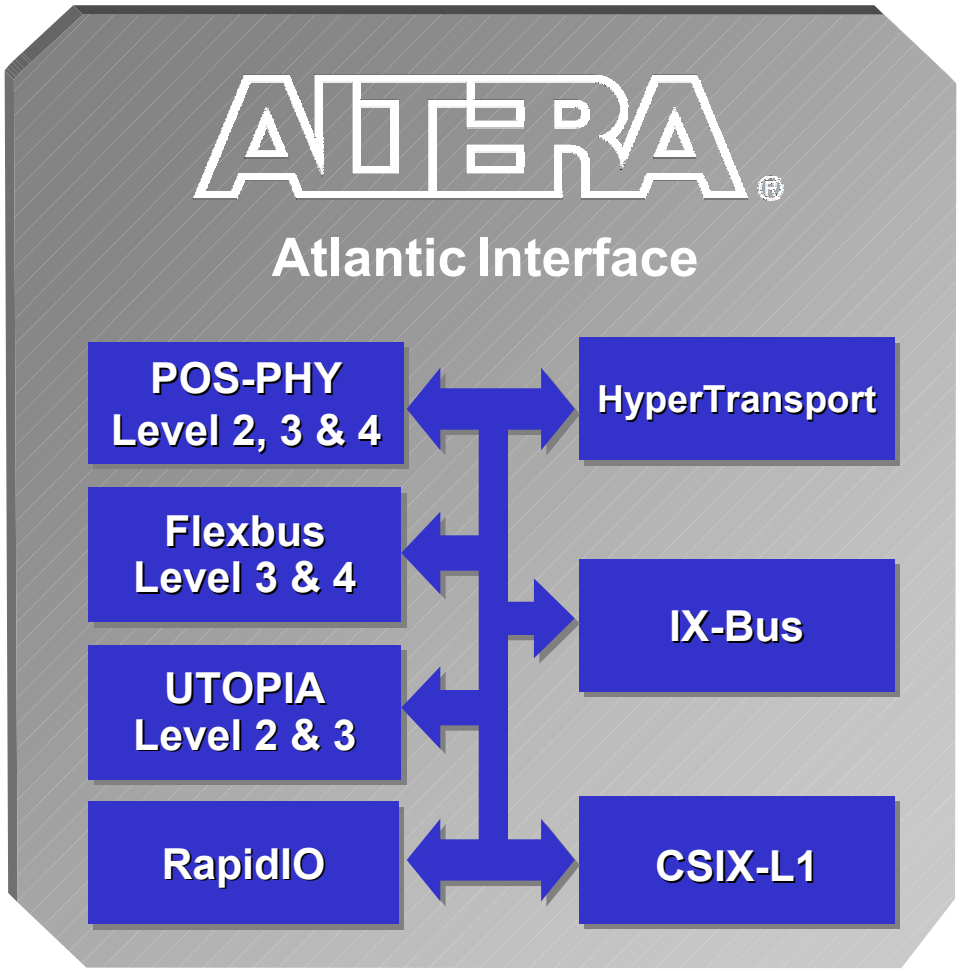
# Atlantic Interface

- Atlantic™ Interface Is an On-Chip PLD Packet-Based Interface
  - Full-Duplex, Synchronous Bus Protocol
  - Enables Seamless Integration Between Interfaces
  - High Performance
  - Easy to Implement
  - Scalable
- Specification Available Today
- Supported by AMPP℠ Partners



# Altera Bridges High-Speed Interfaces

Atlantic




PMC-Sierra
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MOTOROLA

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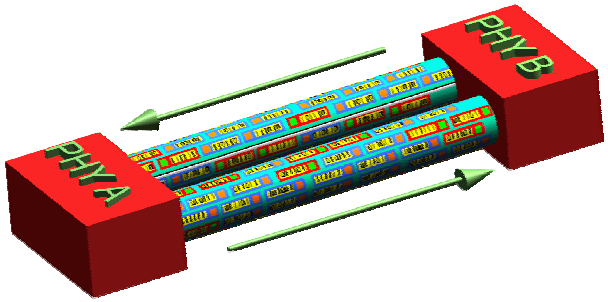
# Altera's HyperTransport Solution

January 23-24, 2002

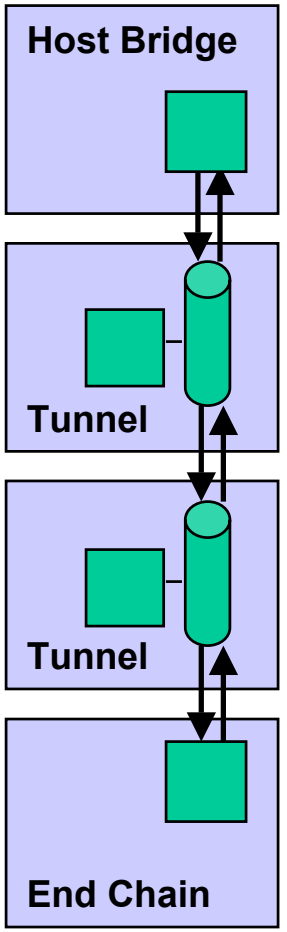
# HyperTransport Functional Overview

- Packet-Based Interface with Two Unidirectional Point-to-Point Links
  - Packets are Multiples of 4 Bytes in Length (Maximum 64 Bytes)
- Data Widths of 2, 4, 8, 16 & 32-Bits
- Data Rates of 400, 600, 800, 1,000, 1,200 & 1,600 Mbps per Channel (Bit)
- HyperTransport Differential Signaling
  - I/O Clocked between 200-MHz & 800-MHz Double Data Rate (DDR)
  - Supported by APEX II Family



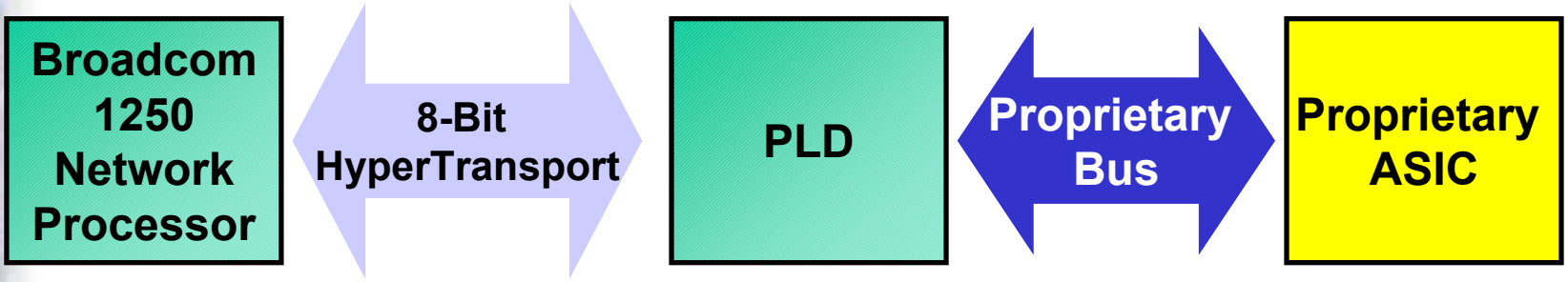
# HyperTransport Topology

- Device Types
  - Host Bridge
  - Tunnel
  - End Chain
- Tunnel & End Chain Devices Cover Majority of PLD HyperTransport Implementations
  - Connecting I/O Devices to HyperTransport Chain
  - Bridging HyperTransport to PCI, Ethernet, SPI-4.2
  - Bridging HyperTransport to Proprietary Buses



# Next-Generation Line Card

- HyperTransport to Proprietary Bus Bridge
  - 8 Bit, 1 Gbps, End Chain

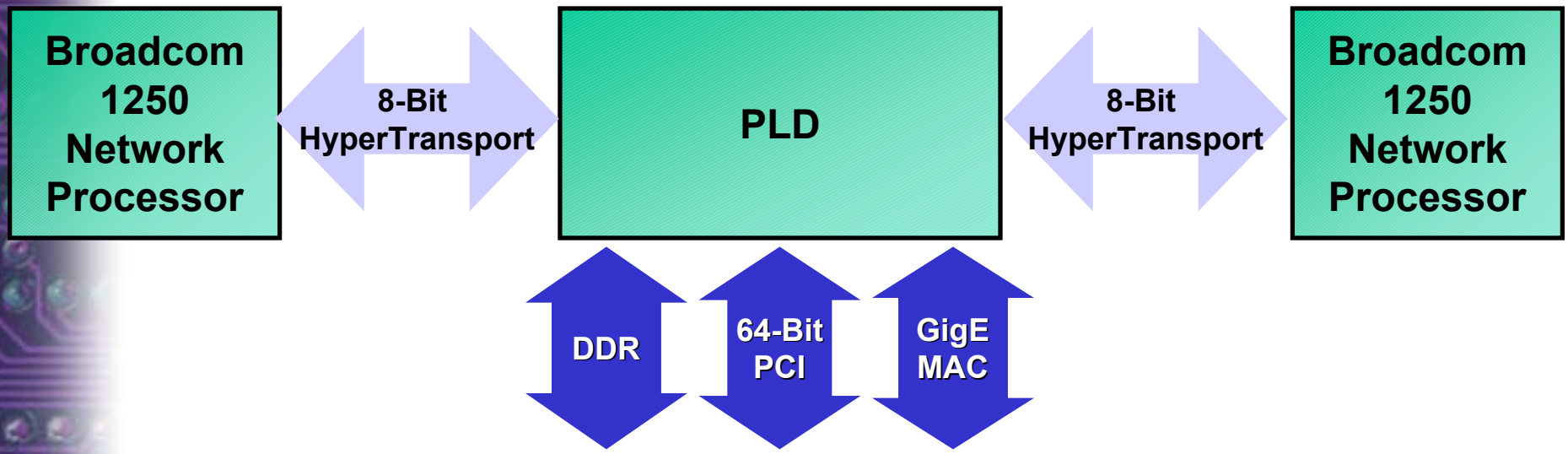


# VoIP Gateway

- HyperTransport to POS-PHY Level 4 Bridge
  - 8 Bit, 800 Mbps, End Chain

# 3G Basestation

- Using PLD for System Integration Simplifies Design
  - 8 Bit, 1 Gbps, Tunnel



# HyperTransport MegaCore® IP Version 1.0.0 Features

- 8-Bit (Roadmap to 16-Bit) Data Width
- 1 Gbps (500-MHz, DDR) per Channel throughput in APEX II Devices
- End Chain Devices (Roadmap to Tunnel)
- Complete HyperTransport Protocol Support
- 128-Bit Data Path, 125-MHz Internal Clock Rate
- Atlantic Local-Side Interface

# HyperTransport MegaCore IP Version 1.0.0 Timeline

- Engaging With Beta Customers Now
- HyperTransport IP Version 1.0.0 Preliminary Release in H1 2002

# Common HyperTransport Applications

- Routers
- Hubs
- Switches
- Servers
- Workstations
- PCs (Desktop & Notebook)
- Set-Top Boxes
- Mobile/Handheld Devices
- Game Consoles
- Embedded Systems


APEX™ II

# APEX II Overview

- **High-Speed I/O Capabilities**
  - 1-Gbps True-LVDS™ Solution, HyperTransport, LVPECL & PCML
  - 624-Mbps, Flexible-LVDS™ Solution, LVPECL & HyperTransport
  - RapidIO, UTOPIA IV, Flexbus CSIX, POS-PHY Level 4
  - 250-MHz HSTL


- **Internal & External Memory Options**
  - 4-Kbit Memory Blocks with Bi-Directional Read / Write Ports
  - External Interface Support for ZBT, DDR & QDR RAMs

- **Maximized Chip-to-Chip Performance**
  - Clock-Data Synchronization
  - 1-Gbps LVDS & LVPECL
  - Up to 124 High-Speed Channels

# APEX II Product Offerings

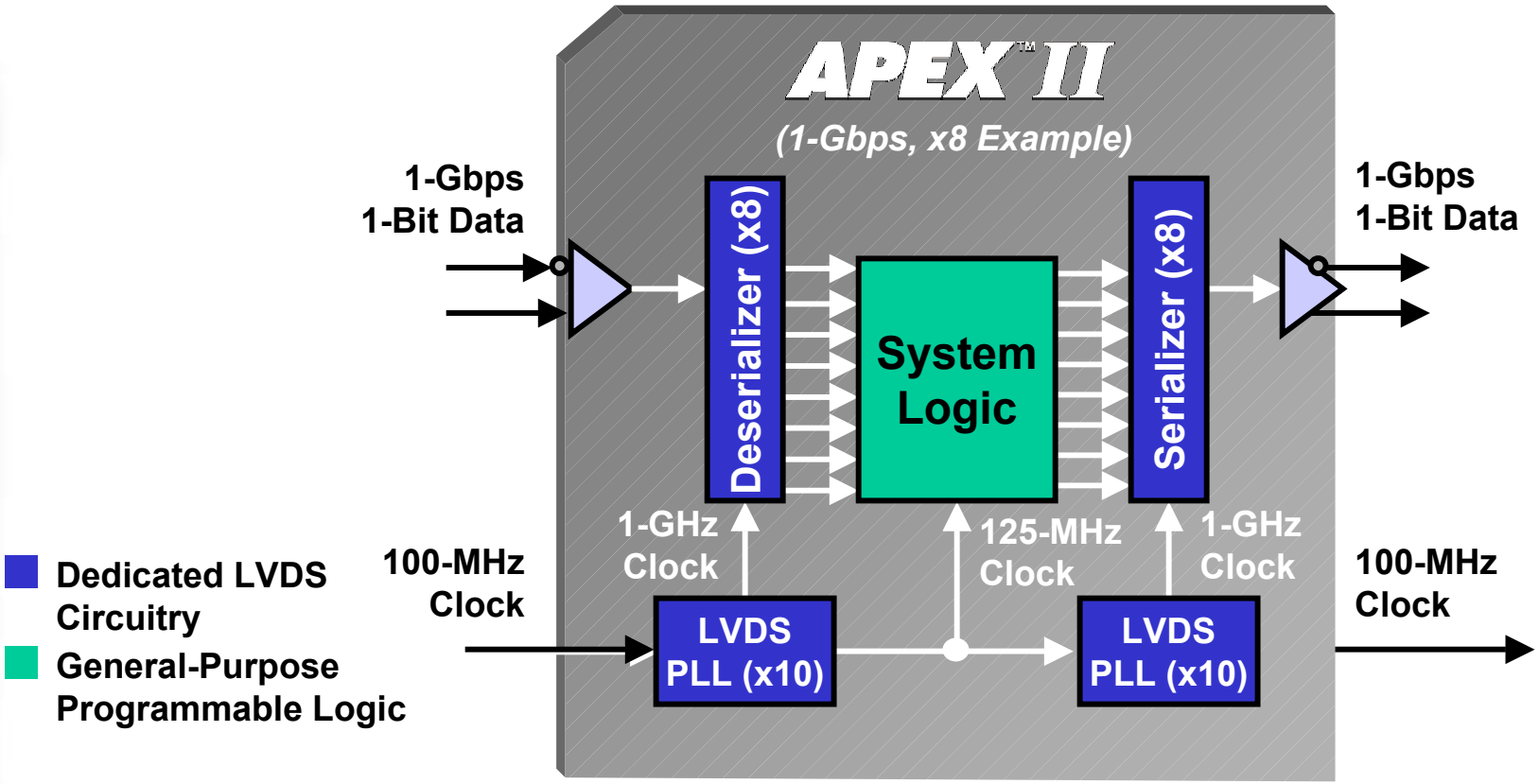
| Device | Logic Elements | RAM Bits | LVDS Channels (Input/Output) | | Max. User I/O Pins |
|---|---|---|---|---|---|
| | | | 1-Gbps True-LVDS* | 624-Mbps Flexible-LVDS** | |
| EP2A15 | 16,640 | 416K | 36 / 36 | 56 / 56 | 492 |
| EP2A25 | 24,320 | 608K | 36 / 36 | 56 / 56 | 607 |
| EP2A40 | 38,400 | 640K | 36 / 36 | 88 / 88 | 735 |
| EP2A70 | 67,200 | 1,120K | 36 / 36 | 88 / 88 | 1,060 |

* True-LVDS Channels Also Support LVPECL, PCML & HyperTransport I/O
** Flexible-LVDS Channels Also Support LVPECL Inputs & HyperTransport I/O

***Devices Available Now!***

# APEX II True-LVDS Circuitry

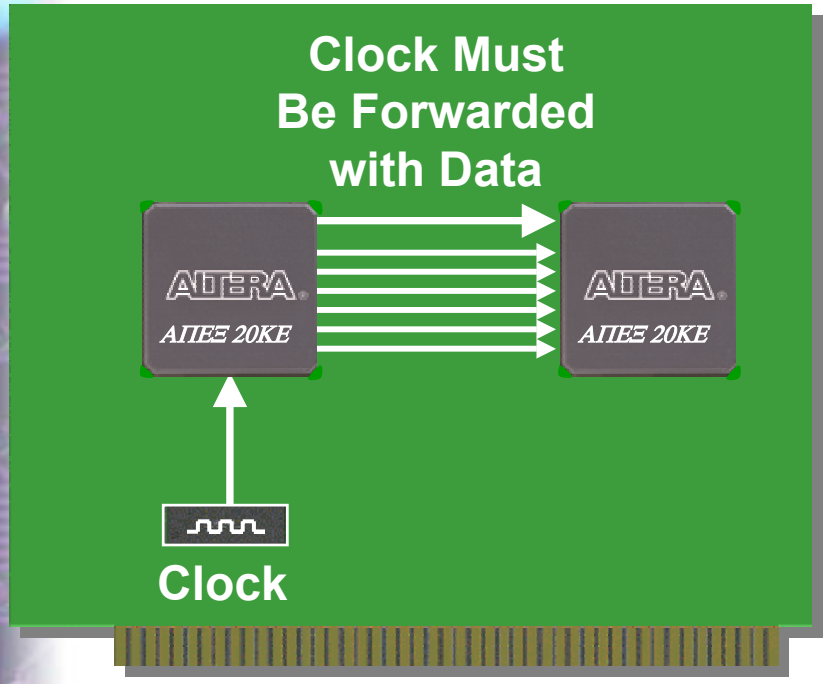
- Dedicated True-LVDS Circuitry Enables 1-Gbps Differential Signaling
- 36 Input & Output Channels per Device
- LVDS, LVPECL, PCML & HyperTransport Support
- Features Two Improved & Independent Clock Domains



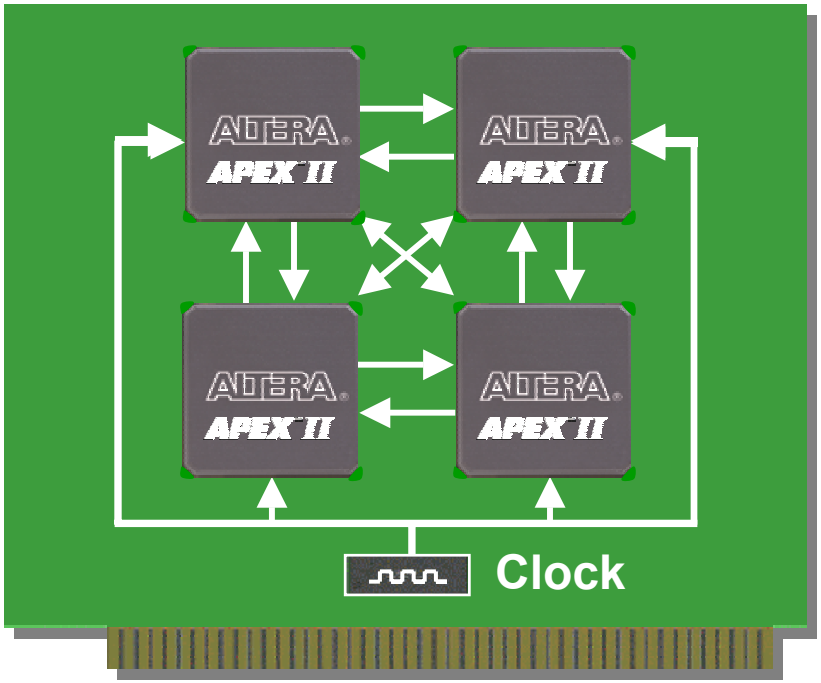
# APEX II Clock-Data Synchronization

- CDS Circuitry Synchronizes True-LVDS Channels to System Clock
  - Performed Independently on All Channels

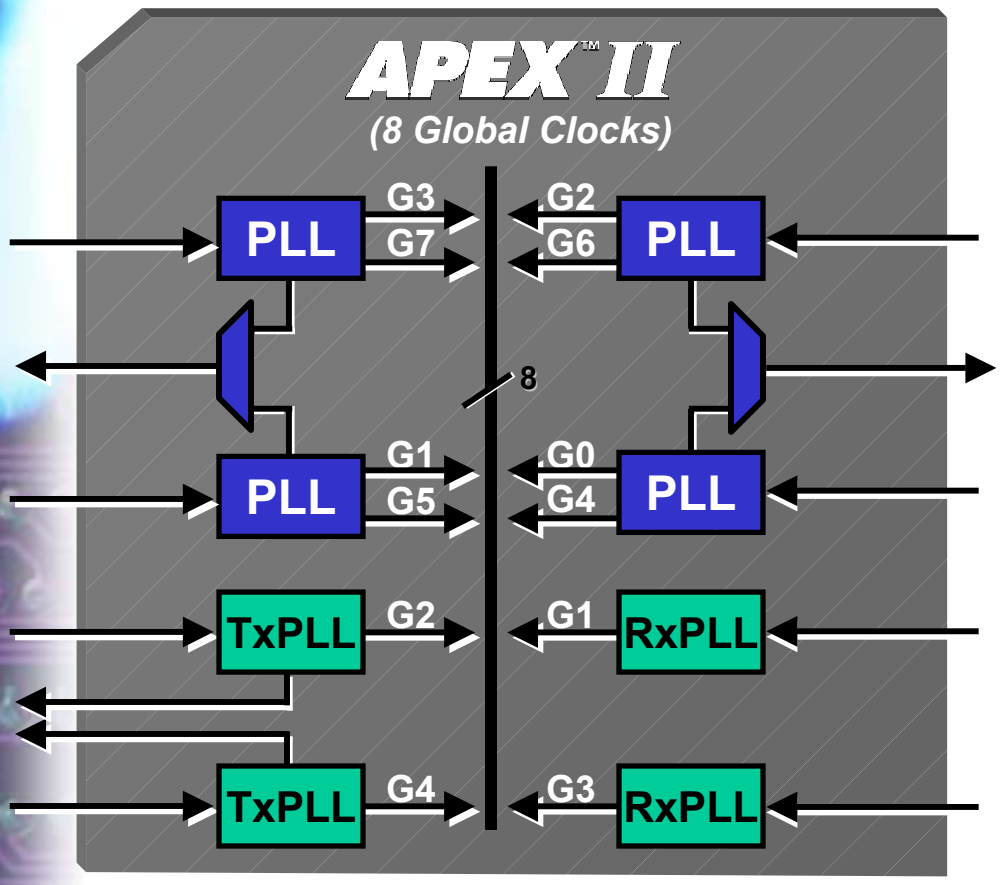
*Source-Synchronous Transfer Limited to Two Devices*




*Chip-to-Chip Transfer with CDS Offers Unlimited Chip-to-Chip Communication*



# APEX II Phase-Locked Loops




| PLL Applications |
| --- |
| True-LVDS |
| Double Data Rate I/O |
| Flexible-LVDS |
| Internal Clock Management |
| Frequency Synthesis |
| External System Clock Management |
| Physical Layer I/O Standards |

General-Purpose PLL

Dedicated LVDS PLL

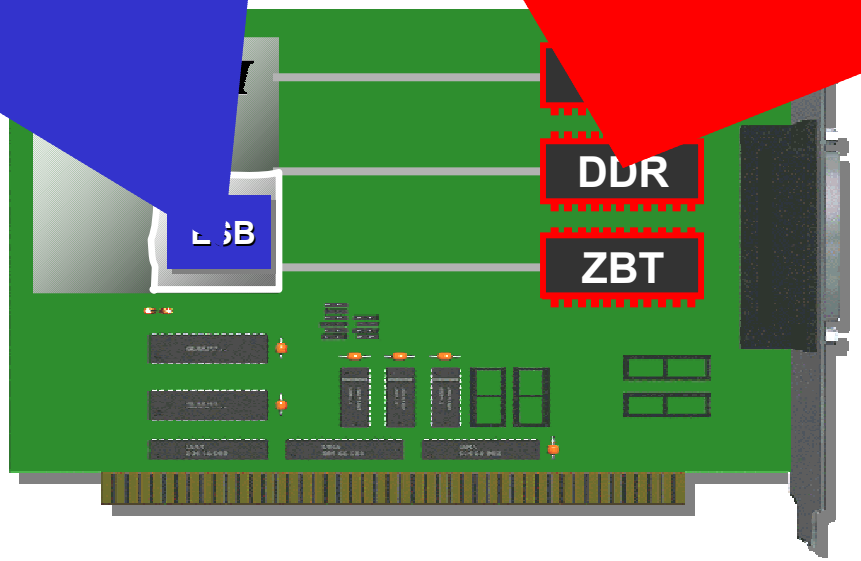
# I/O Standards Supported

| I/O Standard | Performance | Type |
|---|---|---|
| HyperTransport | 1 Gbps | Differential |
| LVDS | 1 Gbps | Differential |
| LVPECL | 1 Gbps | Differential |
| PCML | 1 Gbps | Differential |
| HSTL Class I & II | 500 Mbps | Single-Ended |
| SSTL-2 Class I & II | 332 Mbps | Single-Ended |
| SSTL-3 Class I & II | 332 Mbps | Single-Ended |
| PCI-X | 133 MHz | Single-Ended |

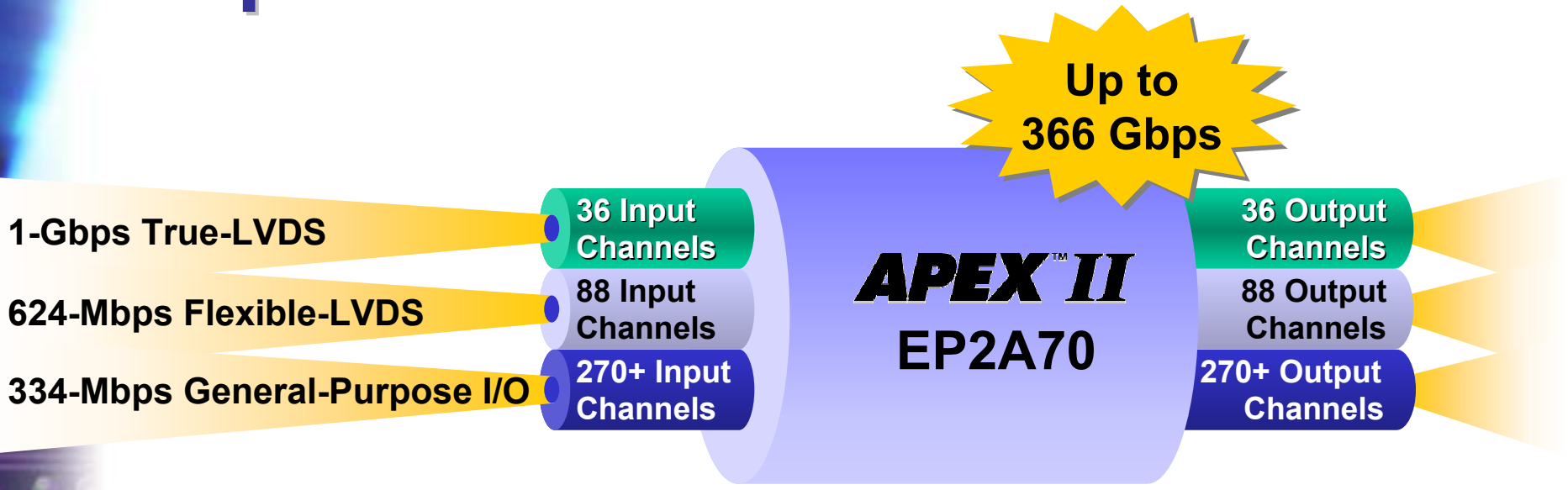
# Complete Memory Solution

| Internal RAM Blocks |
| --- |
| 4 Kbits per Block |
| Dual-Port RAM Mode |
| Packing Mode |
| Mixed Port Widths |

| External Memory Interface | |
| --- | --- |
| Memory Type | Performance |
| ZBT SRAM | 200 MHz |
| SDR SDRAM | 200 MHz |
| DDR SRAM | 334 Mbps |
| QDR SRAM | 668 Mbps |
| DDR SDRAM | 334 Mbps |



# Unparalleled Device Bandwidth




## Compare Device Bandwidths

| | Previously | Today |
|---|---|---|
| Device | EP20K1500E | EP2A70 |
| True-LVDS Bandwidth | 27 Gbps | 72 Gbps |
| Flexible-LVDS Bandwidth | - | 110 Gbps |
| General-Purpose Bandwidth | + 110 Gbps | + 184 Gbps |
| Totals | 137 Gbps | 366 Gbps |

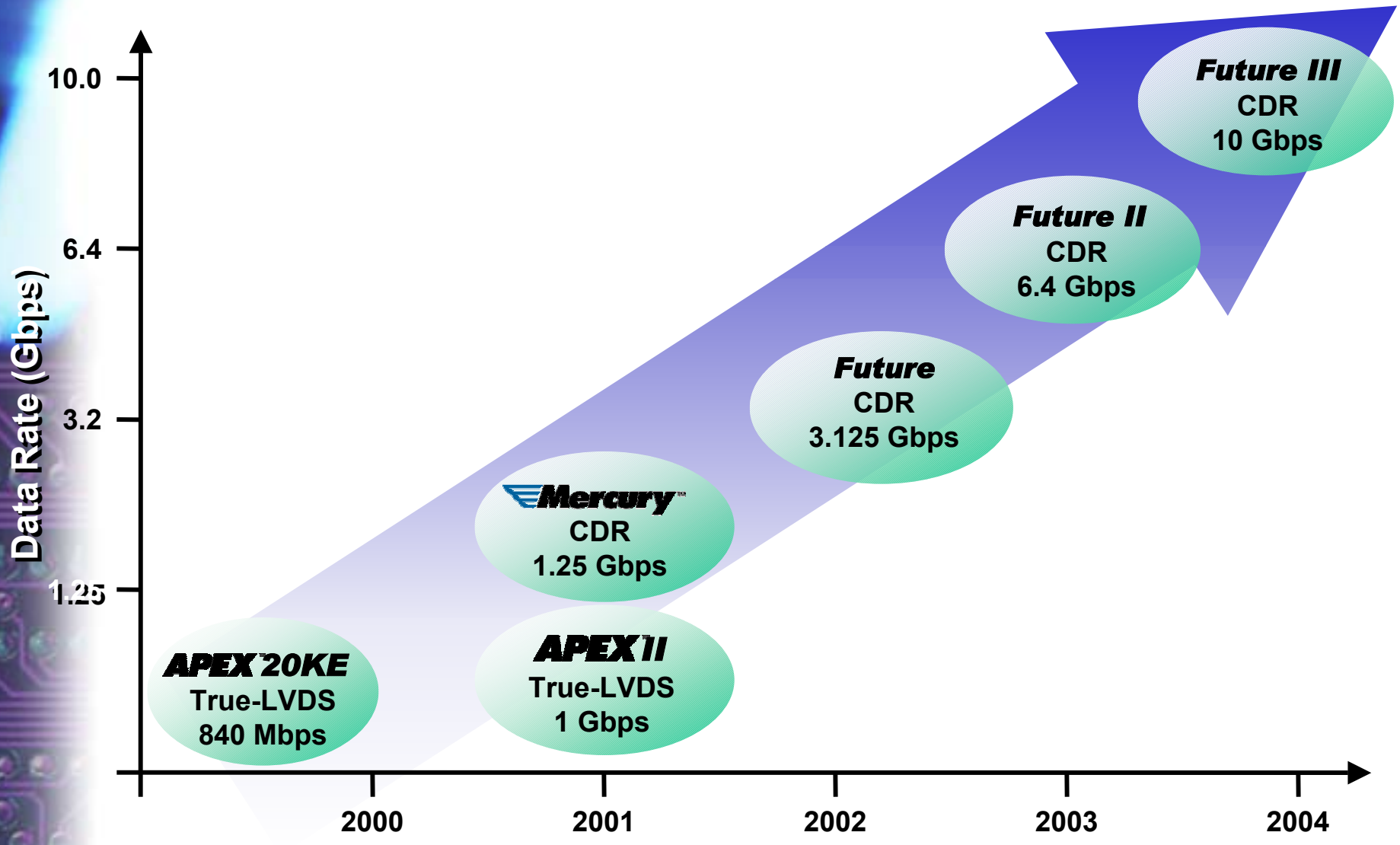
# Interfaces Supported by Altera

| Interface Standard | Bandwidth (Gbps) | Number Of Channels | Needed I/O Performance (Mbps) | I/O Standard | APEX II |
|---|---|---|---|---|---|
| HyperTransport | 16G | 16 + 2* | 1,000 | Hyper-Transport | ✓ |
| UTOPIA IV | 10G | 32 | 416** | LVDS | ✓ |
| RapidIO | 16G | 16 + 1* | 1,000 | LVDS | ✓ |
| POS-PHY Level 4 | 10G | 16 + 1* | 622 | LVDS | ✓ |
| CSIX | 32G | 128 | 250 MHz | HSTL | ✓ |

* Control Signal, ** Overhead Included

# Looking Forward

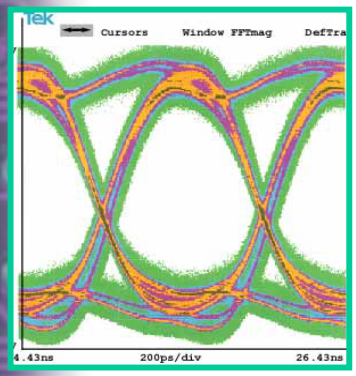
# High-Speed I/O Roadmap



# Proven High-Speed I/O Design Expertise

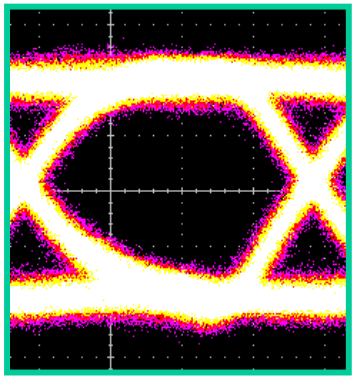
- 2.5-Gbps CDR Test Chip
- 3.125-Gbps Chip in Joint Development

APEX™



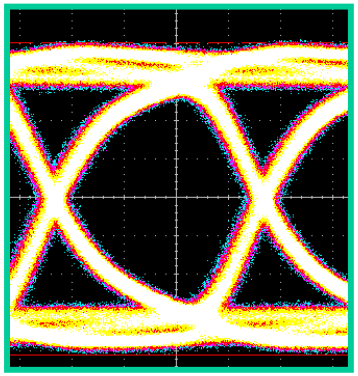

840 Mbps

Mercury™



1.25 Gbps

***Test Chip***



2.5 Gbps

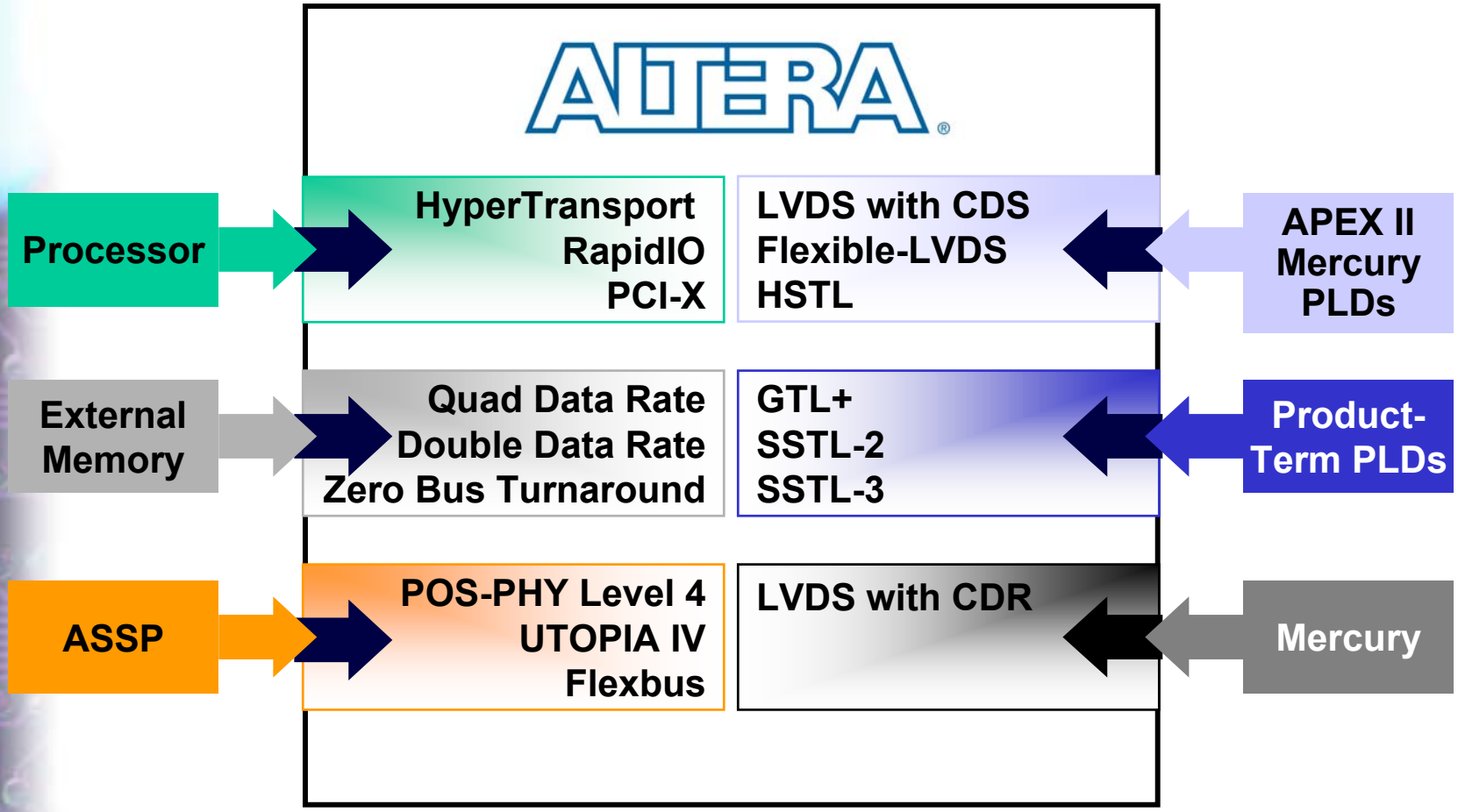
***Next Generation***

***2002***

3.125 Gbps

# Altera's Complete I/O Solution

- Altera Enables High-Speed Communication among Multiple Devices Using Multiple Standards



# Summary

- APEX II Offers a Complete HyperTransport Solution for Today's System Interface Needs
- APEX II Offers the Most Complete I/O for Programmable Logic
- APEX II Has Broadest Differential I/O Support
- We Have the Tools, IP & Tech Support Team to Help Make You Successful

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